**CSE 661**

A) R1 IBM 360

The paper titled “Architecture of the IBM/ 360” discusses the objectives of the design and the key features of IBM/ 360 architecture to serve for the modern technologies and applications that have been gradually evolved. The rationale has been given for the data formats, instruction set and the I/O controls. Along with explaining about the architecture it also tells about the problems that have been encountered to make the system design more compatible.

The design structures were an innovative approach that would be made available to the next decade. A general method was developed for the I/O that make systems specifically available for given applications. The CPU functions were made to be made efficient, and compatible. Machines were made capable of supervising themselves.

The most notable features that were discussed were the relative dependence of the logical structure and physical realization that implements efficiently at various levels of performance, tasks that are catered to a system are common to an operating system requires a complement of instructions and system functions that can be used in future.

Some of the features that were explained that are still in used today are the formulation of an eight-bit system, which paved the way to the inception of byte-addressable memory, the conceptualization of the general-purpose registers against the registers that were dedicated to data and addressing, introduction to ISA.

RISC

The author in this paper “The Case of Reduced Instruction Set Computers” compares the CISC architecture to the RISC architecture and states that increasing the complexity is always not beneficial sometimes it does more harm than good, this was seen in the trend in respect to CISC.

The paper presents the reasons for the increases in the complexity of the systems that were developed, such as speed of memory v/s speed of CPU, Microcode and LSI technology, Code density, Marketing strategy, Upward compatibility, Support of high level languages, use of multiprogramming.

The additional complexity such as difference between speed of memory and CPU, increase in code density to restrict the short comings of less memory in the old computers and the use of High level programming language. is always not cost effective and sometimes might even be of more harmful than good. The author states that the increase in complexity is most common type of architectural change happening over time.

In the paper the author has shown that RISC architecture has certain advantages over the CISC architecture. The unique features that are made for the RISC architecture are implementation feasibility, here in implementation feasibility the complex architecture has a less chance of being realized in a given technology that performs a less complicated architecture. Simple set of instructions are sometimes faster than complex functions. Albeit the construction of CISC architectures takes less time whereas the development time required would be comparatively high and thus makes it unfeasible for development in machines which run on primitive technology which causes the CISC architecture to lag RISC architecture. The above architectural drawbacks can be overcome by using the RISC architecture.

The RISC has the capability to implement the entire CPU design on a single chip, accompanied with the advantage and reduced design, thus makes the RISC architecture more suitable design for the VLSI technology. The processor speed in the RISC architecture still holds good because in the RISC architecture there is a better usage of the chip area and the availability of the modern technology also contributes to the speed. The delay in implementation of the CISC and the advances in the semiconductor devices have clearly given an advantage to the RISC architecture.

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B)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Decade | Year | Frequency(MHz) | Transistor Count | Transistors Rate of change (per decade) | Frequency  Rate of change (per decade) |
| 70 | 1971 | 0.108 | 2300 | 0 | 0 |
|  | 1972 | 0.800 | 3500 | 1.52 | 7.407 |
|  | 1974 | 2 | 4500 | 1.956 | 18.518 |
|  | 1978 | 5 | 29000 | 12.60 | 46.2962 |
| 80 | 1982 | 6 | 134000 | 58.26 | 55.55 |
|  | 1985 | 16 | 275000 | 119.56 | 148.148 |
|  | 1989 | 25 | 1200000 | 521.73 | 231.481 |
| 90 | 1993 | 66 | 3100000 | 1347.82 | 611.11 |
|  | 1995 | 200 | 5500000 | 2391.30 | 1851.85 |
|  | 1997 | 300 | 7500000 | 3260.86 | 2777.77 |
|  | 1998 | 266 | 7500000 | 3260.86 | 2462.96 |
|  | 1999 | 600 | 9500000 | 4130.43 | 5555.55 |
| 00 | 2000 | 1500 | 42000000 | 18260.8 | 13888.89 |
|  | 2001 | 1700 | 42000000 | 18260.8 | 15740.74 |
|  | 2003 | 1700 | 55000000 | 23913.04 | 15740.74 |
|  | 2006 | 2660 | 291000000 | 126521.73 | 24629.629 |
|  | 2008 | 2400 | 410000000 | 178260.86 | 22222.22 |
| 10 | 2010 | 3800 | 1160000000 | 504347.82 | 35185.18 |
|  | 2012 | 2900 | 1400000000 | 608695.65 | 26851.85 |

Table to plot the number of transistors with feature size

|  |  |
| --- | --- |
| Number Of transistors | Feature Size |
| 2300 | 10000 |
| 3500 | 10000 |
| 4500 | 6000 |
| 29000 | 3000 |
| 134000 | 1500 |
| 275000 | 1500 |
| 1200000 | 1000 |
| 3100000 | 800 |
| 5500000 | 350 |
| 7500000 | 250 |
| 9500000 | 250 |
| 42000000 | 180 |
| 55000000 | 90 |
| 291000000 | 65 |
| 410000000 | 45 |
| 1160000000 | 32 |
| 1400000000 | 22 |

Graph representing the number of transistors and the feature size



800 1000 1200 1400 1600

600

400

200

0

12000

10000

8000

6000

4000

2000

0

**Transistor count v/s Feature Size**

EXERCISE

1.a)

Yield = Wafer field \* ((1/ (1+Defects Per Unit area \* Die Area)/N) ^N)

Wafer Field =100%

Defects Per Unit area = 0.3

Die Area = 400mm = 4

N = 5

Yield = 1/ [((1+0.3\*4)/5) ^5]

=1/2.93

=0.3412

b) The process A has lower defect rate than the other because it uses larger transistor feature size.

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2) According to Moore’s Law the number of transistors in dense integrated circuits doubles in 2 years.

Let the number of transistors be “X” in 2015. Then according to Moore’s Law, the number of transistors in the year 2025 would be (2^5) = 32 times.

Therefore by 2025 the number of transistors by 2025 would be “32X”.

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3) Amdhal’s Law

Speed Up overall

= 1/((1-Fraction enhanced)+(Fraction Enhanced/Speedup enhanced))

Overall Speed up with N processors is

=1/(0.5+0.5/N)

Overall Speed up with 1000 processors

SpeedUp

= 1/(0.5+0.5/1000)

= 1.99

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4) Power dissipated = 14 KW= 14\*1000 W

Power of processor P2= 60 W

Power of 240 pin DRAM = 2.3 W

Power of Hard Disk Drive HDD2 @7200 rpm= 7.9 W

Numbers of Servers with Processors = 14\*1000 / (60+2.3+7.9) = 199

------------------------------------------------------------------------------------------------CASE STUDIES

A a)

Cycles per instructions (CPI) = ∑ (CPI \* instructions)

MIPS = (Total number of millions instructions/Total Time)

Let “N” be the total number of instructions

CPI old = (1\*0.3) +( 2\* 0.2) + (3\* 0.4) +( 5\*0.1)

=0.3+0.4+1.2+0.5

=2.4 CPI

MIPS old = N/((2.4\*N\*10^6)/ 400\*10^6) = 166.67

CPI new = (1\*0.3) +( 2\* 0.2) + (3\* 0.4) +( 13\*0.1)

=0.3+0.4+1.2+1.3

= 3.2 CPI

MIPS new = N/((3.2\*N\*10^6)/400\*10^6) =125

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A b) Die Yield = Wafer field \* (1/ (1+Defects Per Unit area \* Die Area) ^N)

Yield old = 0.75 \*(1/ (1+2\*0.12) ^4)

=0.317

Yield new = 0.75\*(1/ (1+2\* 0.10) ^4)

=0.361

Die per Wafer is given by the formula:

Dies per Wafer = (π\*(waferdia/2)/Die Area) –(π\*(waferdia)/ √ (2\*Die Area))

Wafer dia = 10cm

Wafer Dia old = π\*(10/2) ^2/0.12 – π\*10/√ (2\*0.12)

= 654.166-64.09

= 590.07

Wafer Dia new = π\*(10/2) ^2/0.1 – π\*10/√ (2\*0.1)

= 715.15

Cost of a single die is,

Cost of Die = (Cost of Wafer/Die yield\* Die per Wafer)

Cost old = (1000/(0.317\*590.07))

= 5.3475

Cost new = (1000/ 0.361\*715.15)

= 3.83

The cost of the die earlier before was $5.3475 and after the changes it has gone down to $ 3.83.

The reduced in the prices is due to the increase in the die yield and die per wafer.

Since the total time to execute the statements has increased, the performance has also gone down.

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A c) The best possible speed that could be achieved theoretically is “infinity” by considering the infinite parallelism. So the effective clocks for FP would be Zero.

Speed up =1/((1-f) +(f/N)

f= CPI of FP/Total CPI

= 0.10\*5/2.4

= 0.208

Speed up = 1/ (1-0.208)+0.208/∞)

=1/ (0.792)

= 1.262

Speedup =execution time(old)/Execution time(new)

1.262=2.4/CPI

=>CPI= 1.907

MIPS= clock rate/CPI\*10^6

= 400\*10^6/1.907\*10^6

= 209.75

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B) The relation between power, Energy and time is given as

Power(P) = Energy(E)/Time(T)

According to the relation the reduction 20% in the clock time, would cause the processor to run slower, which in turn consumes more time to complete an operation. This will result in less power being consumed as the clock is directly proportional to the power consumed.

Therefore, as the energy consumed is a function of both power and time, therefore a decrease in clock will cause less power to be consumed but will also result in additional time consumed to complete the given task.

Hence, there will be no effect on the battery life of the mobile device.

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